(12) UK Patent Application (19) GB (11) 2 214 759 (13) A

(43) Date of A publication 06.09.1989

(21) Application No 8801036.8

(22) Date of filing 18.01.1988

(71) Applicant
The Plessey Company plc

(Incorporated in the United Kingdom)

Vicarage Lane, Ilford, Essex, IG1 4AQ, United Kingdom

(72) Inventors
Ian Robert Patient
Anthony Peter Hulbert
John Joseph Spicer

(74) Agent and/or Address for Service
E Pritchard
The Plessey Company plc, Intellectual Property Department, Vicarage Lane, Ilford, Essex IG1 4AQ, United Kingdom

(51) INT CL'
H04L 1/00, G06F 11/10, H03M 13/00 // G11B 20/18

(52) UK CL (Edition J)
H4P PEP
U1S S2100 S2117

(56) Documents cited

GB 2060227 A	GB 2048529 A	EP 0201088 A2
EP 0006480 A1	WO 81/02352 A	US 4700350 A
US 4677625 A	US 4649541 A	US 4455655 A

(58) Field of search
UK CL (Edition J) G4A AED AEE APP, H4P PEP PEX
INT CL' G06F 11/10, G11B 20/18, H03M 13/00, H04L 1/00

(54) High speed digital data link

(57) A high speed digital data link includes a convolutional code encoder 7 arranged for generating blocks of coded data for transmission through a channel, the link including means 9 for receiving said coded data, a plurality of decoder input buffer 16 means each with an associated decoder 11, a switch being arranged to direct data blocks of the data stream to each of the buffer and decoder combinations in turn, the switch operation being arranged such that the contents of one buffer at any time have a slight overlap with the contents of the next buffer in sequence, (Fig 3).

This can allow an encoder of simple construction to be used which thus makes the link particularly suitable for satellite communication. Storage or recording of data are also envisaged.

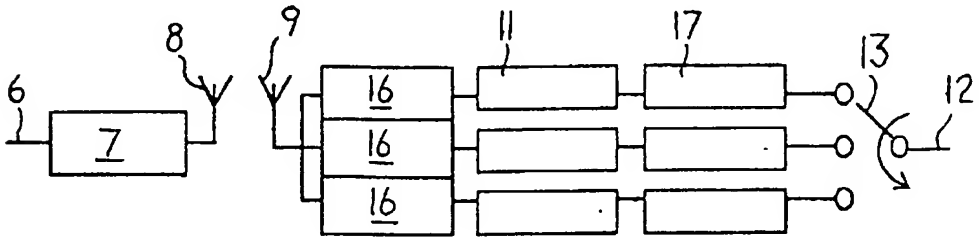

Fig.1

GB 2 214 759 A

2214752

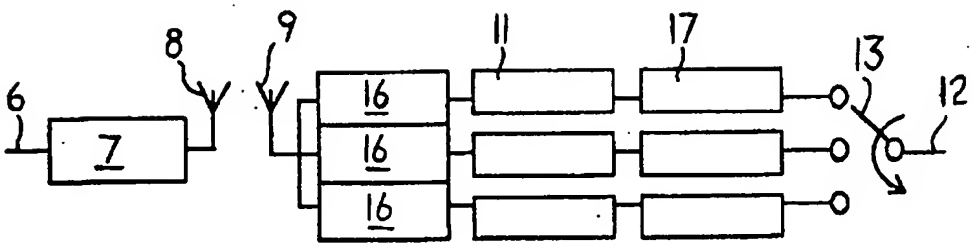

Fig.1

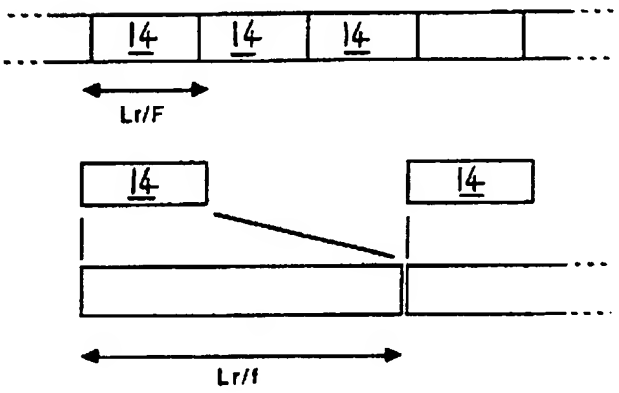

Fig.2

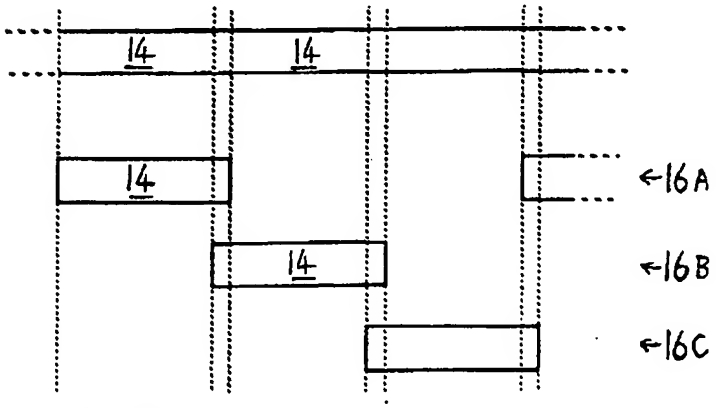

Fig.3

2214759

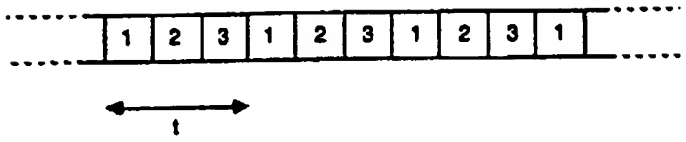

Fig.4

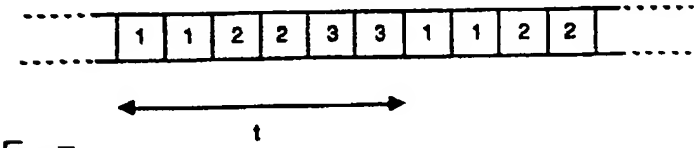

Fig.5

HIGH SPEED DIGITAL DATA LINK

This invention relates to a high speed digital data link.

The high speed transmission of data has become an important subject in recent years, with the emergence of data networks for the exchange, processing and storage of digital information. In order to transmit the information in the presence of a possibly noisy channel or storage medium, it has been shown that a proper encoding process applied to the message material, can enable the errors to be reduced without sacrificing the rate of information transmission or storage. The use of coding therefore has become an integral part in the design of modern communication systems and digital computers.

There are two different types of codes in common use today, block codes and convolutional codes. The present invention relates to a data link for the convolutional type of code and this requires a code encoder part of the data link to include a memory arranged so that the encoder outputs at any given time unit depend not only on the inputs at that time unit but also on previous input blocks.

Convolutional codes are designed to combat the effects of channel errors. The information to be transmitted is transformed by the encoder. This transformation also adds enough redundancy (derived from the input information) to the encoder output for a decoder to be able to estimate what had actually been sent in the event of corruption of data between encoder and decoder as a result of any channel errors. To ensure more effective performance a further protection can be introduced. Both the transformation and the redundant data can depend on the information given to the

encoder up to several transformations earlier. That is, the encoder has memory.

Where the expected data rate is as high as several hundred mega-bits per second, it is desirable to have several decoders operating at a lower speed. It is also possible to have several encoders, so that the original data is multiplexed to the encoders, their outputs being interleaved, transmitted, and multiplexed to the decoders.

According to the invention, a high speed digital data link includes a convolutional code encoder arranged for generating blocks of coded data for transmission through a channel, the link including means for receiving said coded data, a plurality of decoder input buffer means each with an associated decoder, a switch being arranged to direct data blocks of the data stream to each of the buffer and decoder combinations in turn, the switch operation being arranged such that the contents of one buffer at any time have a slight overlap with the contents of the next buffer in sequence.

Each data output lead from the decoders may be connected to a decoder output buffer, if required. Conveniently, the decoder output buffer output leads are connected to a further switch to provide a stream of interleaved buffer outputs on a common output line, the switch serving to connect the next buffer when one buffer has been emptied.

By way of example, some particular embodiments of the invention will now be described with reference to the accompanying drawings, in which:

Figure 1 is a block diagram of a digital data link having an encoder and a decoder,

Figure 2 shows a stream of data input bits as they enter the decoder,

Figure 3 is a diagram showing the principle of operation of an overlapping buffer arrangement,

Figure 4 shows an example data stream entering the encoder, and,

Figure 5 shows an example data stream as received at the decoder of the data link.

For a high speed digital data link it is desirable to make use of several data decoders for the transmitted information, these decoders operating simultaneously and their individual speed of operation can then be somewhat less than the speed of the incoming data stream. Such an arrangement is depicted in Figure 1 where the digital data link comprises an information source output line 6 which is connected to an encoder 7. Data from the encoder 7 is delivered to a transmitter aerial 8 for reception by a receiver aerial 9. The transmitter aerial 8 and receiver aerial 9 form part of a communications channel which is likely to be subject to noise and interference which will affect the accuracy of the data signals arriving at the aerial 9.

The receiver aerial 9 is connected to a decoder 11. The decoder 11 provides a stream of signals on a data output line 12.

In order to be able to cope with a very high speed of data transmission, the decoder 11 represents a bank of similar decoders which are connected in parallel and which can be fed in sequence

with the incoming data. A switch 13 at the output end of the decoder serves to connect the outputs in turn to the data line 12.

Figure 2 shows the blocks 14 of digital data as they are received in series at the aerial 9. The middle portion of Figure 2 shows the length of a single block 14 (which is proportional to time) allowing a small extra time interval at each end of the block for an overlap portion. The lower part of Figure 2 shows the time that would be taken to process this single block of data by one of the decoders 11.

There is thus a problem in decoding the transmitted data blocks 14 which is due to the available speed of operation of the decoder 11. The problem can be overcome by providing a bank of the decoders 11 and feeding successive data blocks 14 to each of these decoders in sequence. A decoder input buffer 16 (Figure 1) can serve to hold each data block while its decoder 11 decodes the buffer contents. Thus a data block which has arrived earlier at that decoder can be properly processed before the next block arrives.

Figure 2 shows an arrangement in which the time taken to process each block is about three times (for example) the length of a single block. Three buffers 16A, 16B and 16C (Figure 3) will be sufficient to hold each successive data block whilst its decoder 11 decodes the buffer contents. This arrangement will thus give continuous decoding of all the data blocks in the stream together with the small overlap portions at the beginning and end of each block.

At the output ends of the decoders 6, decoder output buffers 17 can be provided to hold the output signals so that after one buffer

has delivered its output through the switch 13 the switch can be moved so the next buffer can deliver its output to the data output line 12.

In operation of this system, the decoders are used to process consecutive blocks of data independently by overlapping their domains. This gives the decoders an opportunity to align themselves before being required to give valid data. There is no need to extract any block synchronisation information from the received code bit stream.

Figure 4 depicts a stream of data input bits, as they are received at the switch before the encoder 7. Each bit is marked with the number of an encoder 7 to which it is intended to go. A complete cycle of operation of the switch occurs in the time t.

Figure 5 shows a stream of transmitted bits as they leave the encoder 7. Each bit is marked with the number of the encoder from which it comes.

The decoder continually updates its model of the succession of states of the encoder. It therefore needs a significant amount of received code data in order to form a reliable estimate of what was originally sent. Thus, no reliable estimate of what has just been sent is available until some time later. In addition, if the decoder starts work on a data stream in mid flow, not starting from a known encoder state, it needs a finite quantity of received code data in order to be able to estimate the encoder state. Data generated in this start-up time is not reliable.

An example of a digital data link that was designed had the following performance parameters:

By definition, F = channel information data rate, bits per second

n = number of decoders

f = decoder output data rate, bits per second

L = block length, equivalent number of information bits, not including overlap required

r = overlap factor (block length including overlap is rL)

R = code rate

Code data from the encoder is transmitted at a rate of L/RF bits per second.

To determine the number of decoders required, note that a block length (including overlap) must be processed before (n-1) more blocks (without overlap) are received (see Figure 2), that is $n(L/F) > rL/f$, thus $n > Fr/f$

The delay due to this arrangement is thus about Lr/f or nL/F.

In a numerical example,

Code Parameters

Code rate	1/2	R
Code constraint length	7 (=14 code bits)	

Data Rates

Data rate	150 Mbps	F
Transmission rate	300 Mbps	

Decoder capability

Reception rate	30 Mbps	
Output rate	15 Mbps	f

System Requirements

Data delay less than 100μs

These conditions will be satisfied with

L	block length (in equivalent information bits) (without overlap)	1400
r	overlap factor (found assuming 5 constraint lengths required overlap at each end of block)	1.05
n	number of decoders	11

It is typical that the number of decoders required is just larger than the ratio of the speeds of the encoder and decoders.

Thus each decoder input buffer will accept 2*(1400+70)=2940 code bits, overlapping 2*(70)=140 code bits with previous and following buffers each. The first 70 bits in the buffer will be used to estimate the encoder state; the rest of the data will generate 1400 information bits for the decoder output buffer to store. Each decoder will take 98.7 μs to process each block of data.

The invention of the present application has been found to provide a useful high speed digital data link which can be used for example for satellite communication. For this purpose, it is desirable to use an encoder of simple construction in the satellite vehicle and this is provided by the arrangement of the present invention. However, it is not essential that the communication channel should be a radio link. A storage medium, for example, provides an alternative channel that can be subject to noise and the need to

convey accurate data to a destination is equally relevant for recorded data.

The foregoing description of an embodiment of the invention has been given by way of example only and a number of modifications may be made without departing from the scope of the invention as defined in the appended claims. For instance, it is not essential that the number of decoders used should be restricted to three. In one particular proposed application, the use of fifteen decoders has been suggested.

CLAIMS

1. A high speed digital data link comprising a convolutional code encoder arranged for generating blocks of coded data for transmission through a channel, the link including means for receiving said coded data, a plurality of decoder input buffer means each with an associated decoder, a switch being arranged to direct data blocks of the data stream to each of the buffer and decoder combinations in turn, the switch operation being arranged such that the contents of one buffer at any time have a slight overlap with the contents of the next buffer in sequence.

2. A data link as claimed in Claim 1, in which each data output lead is connected to a decoder output buffer.

3. A data link as claimed in Claim 2, in which the decoder output buffer output leads are connected to a further switch to provide a stream of interleaved buffer outputs on a common output line, the switch serving to connect the next buffer when one buffer has been emptied.

4. A data link as claimed in any one of Claims 1 to 3, in which said code encoder is formed by a bank of encoders which are connected to a common switch.

5. A high speed digital data link substantially as hereinbefore described with reference to any one of the accompanying drawings.

6. A method of decoding digital data substantially as hereinbefore described.

Published 1989 at The Patent Office, State House, 66/71 High Holborn, London WC1R 4TP. Further copies may be obtained from The Patent Office Sales Branch St Mary Cray, Orpington, Kent BR5 3RD. Printed by Multiplex techniques ltd, St Mary Cray, Kent, Con. 1/87